4th IKEEE-HCMUTE Joint Workshop

January 15-17, 2019
Meeting Room 2, 6th floor, Main Building
University of Technology and Education, Hochiminh City, Vietnam
(https://isdlute.wordpress.com/)

Co-organized by

Institute of Korean Electrical and Electronics Engineers (IKEEE), Korea
Department of Electrical and Electronics Engineering. University of Technology and Education,
HCMC, Vietnam (FEEE-HCMUTE)

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Nguyen Chi Nhan (University of Science, HCMC, Vietnam)
Kyeong-Sik Min (Kookmin University, Seoul, Korea)

INVITED SPEAKERS

Jongsun Kim (Hongik University, Seoul, Korea)
Yong Moon (Soongsil University, Seoul, Korea)
Minkyu Song (Dongguk University, Seoul, Korea)
Jeongjin Roh (Hanyang University, Ansan, Korea)
Kwang-Hyun Baek (Chung-Ang University, Seoul, Korea)
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Pham The Bao (Sai Gon University, HCMC, Vietnam)
Nguyen Chi Nhan (University of Science, HCMC, Vietnam)
Kyeong-Sik Min (Kookmin University, Seoul, Korea)

Jan. 15, 2019 (Tue)	
5:00-7:00 PM	Reception dinner (Hosted by IKEEE)
Jan. 16, 2019 (Wed)	
2:00–6:00 PM	Workshop committee meeting (Hosted by HCMUTE) -Discuss the program and speakers of Joint workshop in 2020 -Discuss the new committee members of Joint workshop in 2020 -Discuss the finance of Joint workshop in 2019
Jan. 17, 2019 (Thu)	
12:00-1:00 PM	Registration and Lunch
1:00-1:10 PM	Opening Ceremony, Assoc. Prof. Hieu Giang Le Vice President of University of Technology and Education, HCMC, Vietnam
1:10–1:30 PM	Design of a LowNoise CMOS Image Sensor with a Fully Differential Difference Amplifier and a Hybrid Column Calibration Technique. (Minkyu Song, Dept. of Semiconductor Science, Dongguk University, Seoul, Korea)
1:30–1:50 PM	High-Performance Low-Dropout Regulators for Mobile Power Management Systems (Jeongjin Roh, Department of Electrical Engineering, Hanyang University, Ansan, Korea)
1:50-2:10 PM	A Design of Rectifier for Wireless Power Transfer (Yong Moon, School of Electronic Engineering, Soongsil University, Seoul, Korea)
2:10-2:30 PM	Design of a Fast-Locking All-Digital Frequency Synthesizer for Fractional-Ratio Dynamic Frequency Scaling (Jongsun Kim, School of Electronic and Electrical Engineering, Hongik University, Seoul, Korea)
2:30-2:45 PM	Coffee Break with Poster Presentation
2:45–3:05 PM	Low-Power Small-Area Direct Digital Frequency Synthesizers (Kwang-Hyun Baek, School of Electrical and Electronics Engineering, Chung-Ang Univ., Seoul, Korea)
3:05-3:25 PM	A Survey on Memristor Circuits and Systems for Brain-Inspired Computing (Son Ngoc Truong, University of Technology and Education, HCMC, Vietnam)
3:25-3:45 PM	A Novel Memristor Crossbar Architecture Based Multilayer Neural Network for Speech Recognition (Minh Huan Vo, University of Technology and Education, HCMC, Vietnam)
3:45-4:05 PM	Parking Space Detection upon a Deep CNN and Multi-task Contrastive Network Spatial Transform (Vu-Hoang Tran, University of Technology and Education, HCMC, Vietnam)
4:05-4:20 PM	Coffee Break with Poster Presentation
4:20-4:40 PM	Innovative Assessment Metrics for Upper Limb Robot-Assisted Rehabilitation (Tran Vi Do, University of Technology and Education, HCMC, Vietnam)
4:40-5:00 PM	Control System with Smart Phone for the Mini Aquaponics Cabinet (Nguyen Van Hieu, University of Science, HCMC, Vietnam)

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5:00-5:20 PM	Coronary Vessel Segmentation by Coarse-to-Fine Strategy using Otsu Algorithm and Decimation-Free Directional Filter Bank (Pham The Bao, Sai Gon University, HCMC, Vietnam)
5:20-5:40 PM	Wireless Sensor Networks for the Internet of Things (Nguyen Chi Nhan, University of Science, HCMC, Vietnam)
5:40-6:00 PM	Thermal Energy Harvesting Circuit for Wearable Applications (Kyeong-Sik Min, School of Electrical Engineering, Kookmin University, Seoul, Korea)
6:00-8:00 PM	Closing Ceremony & Banquet

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Design of a LowNoise CMOS Image Sensor with a Fully Differential Difference Amplifier and a Hybrid Column Calibration Technique

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A low noise CMOS Image Sensor (CIS) based on a fully differential difference amplifier and a hybrid self-calibrated column technique is proposed. Conventionally, the operating speed of a two-step single-slope ADC is faster by about 10 times than that of a single-slope ADC. However, it has a serious connection error between the coarse block and the fine block. Thus a new fully differential difference amplifier is proposed in order to improve the drawbacks of two-step single-slope ADC. Further, a self-calibrated column technique to adopt both an analog calibration block and a digital calibration block is also discussed. With a Samsung 0.13μm CIS technology, a test chip with the proposed techniques has been fabricated. The measured power consumption is about 98uW per column with the high frame rate of 120 frames/s (fps) at the VGA resolution. The measured pixel fixed pattern noise is about 0.43LSB which is much lower than the other conventional techniques.

Minkyu Song received the B.S. and M.S., and Ph.D. degree in Electronics Engineering from Seoul National University, Korea in 1986, 1988 and 1993, respectively. From 1993 to 1994, he was a researcher at Asada Lab., VDEC, University of Tokyo, Japan where he worked in the area of low power VLSI design. From 1995 to 1996, he was a researcher in the CMOS Analog Circuit Design Team of Samsung Electronics, Korea. Since 1997, he has been a professor at University of Dongguk, Korea. He is a member of IEEE and IEIE. His major interest is design of CMOS analog circuits, mixed-mode circuits, and CMOS image sensor.

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High-Performance Low-Dropout Regulators for Mobile Power Management Systems

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Low-Dropout (LDO) regulators are important block for battery-powered mobile devices. The power efficiency is the key factor for long battery life. The switching power converters are used for high power efficiency, but the last stage of the power converters are usually the linear regulators for the sensitive analog circuits. The power supply rejection ratio (PSRR), fast response are important characteristics for the regulators. The development of LDOs for this purpose are discussed in this paper.

Two examples of LDOs are demonstrated. The fast-transient capacitor-less low-dropout (CL-LDO) regulator for system-on-chip applications. A low-quiescent-current class-AB amplifier with embedded slew-rate enhancement circuit is applied to improve transient performance. The enhancement circuit eliminates the need for any additional sensing circuit, and a minimum hardware overhead is required for just the driving circuit. The proposed CL-LDO regulator is fabricated in a 0.18-um standard process. It consumes a quiescent current of 10.2 uA. It can deliver a maximum load current of 100 mA. Another one shows an output-capacitorless, LDO voltage regulator with improved load regulation and fast recovery time was realized using two amplifiers, which provided high gain, high bandwidth, and high slew rate. In addition, a one-shot current boosting circuit was added for current control to charge and discharge the parasitic capacitance at the power transistor gate during the load-current transition to further improve the response time. The experimental results show that the LDO consumes extremely low quiescent current of 4.5-μA.

Jeongjin Roh received the B.S. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 1990, the M.S. degree in electrical engineering from The Pennsylvania State University, State College, PA, USA, in 1998, and the Ph.D. degree in computer engineering from the University of Texas at Austin, Austin, TX, USA, in 2001. He was with Samsung Electronics, Kiheung, South Korea, as a Senior Circuit Designer of Mixed-Signal Products, from 1990 to 1996. He was with Intel Corporation, Austin, as a Senior Analog Designer of Delta-Sigma Data Converters, from 2000 to 2001. He joined Hanyang University, Ansan, South Korea, as a Faculty Member. His current research interests include power management circuits and oversampled delta-sigma converters.

A Design of Rectifier for Wireless Power Transfer

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WPT(Wireless Power Transmission) technology means the transmission of power without physical connection. In this study, a rectifier for WPC/A4WP WPT is designed. It supports both WPC (Wireless Power Consortium) and A4WP (Alliance for Wireless Power) and is designed as full-bridge type. The WPC transmits power at the frequency of 100kHz to 205kHz and the A4WP at the frequency of 6.75MHz. Since the bridge rectifier uses a MOSFET instead of a diode, the reverse current flows and the efficiency is lowered if the output voltage is higher than the input voltage. Therefore, we added a reverse current detector that detects the current flowing through the MOSFET and limits the reverse current. The frequency discriminator is used because two different frequency bands are used. The proposed rectifier was designed using 350nm high voltage CMOS process. The input voltage is up to 18V and the operation frequencies are 100kH ~ 205kHz and 6.78MHz. The maximum efficiency is 94.7% and the maximum delivered power is 5.78W.

Yong Moon received the B.S., M.S., and Ph.D. degrees from the department of Electronics Engineering, Seoul National University, Seoul, Korea, in 1990, 1992 and 1997, respectively. From 1997 to 1999, he was with LG Semicon co., Ltd., where he contributed to senior research engineer in analog circuit design group. Since 1999, he has been with Soongsil University, Seoul, Korea, where he is a professor in School of Electronic Engineering. He was a visiting professor at University of California, Santa Cruz, from August 2012 to July 2013. Prof. Moon served on various technical program committees such as Asian Solid-State Circuits Conference (A-SSCC), International SoC Design Conference (ISOCC), and Korean Conference on Semiconductors (KCS). He and his students received ISOCC design Award in 2014 and 2015. He is a member of Institute of Electrical and Electronics Engineers (IEEE) and Institute of Electronics Engineers of Korea (IEEK). He is the chair of IEEE Solid-State Circuit Society (SSCS) Seoul Chapter since 2016 and served as the organizing vice-chair of A-SSCC 2017. His research interests include PLL, ultra-low power circuit design, NFC/RFID circuit & systems, wireless power transfer circuits, meta-materials and RF circuits.

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Design of a Fast-Locking All-Digital Frequency Synthesizer for Fractional-Ratio Dynamic Frequency Scaling

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A new all-digital multiplying delay-locked loop (MDLL) is presented that can provide programmable fractional-ratio frequency synthesis of de-skewed clock. The proposed fractional-ratio MDLL (FMDLL) employs a new select logic for controlling three operation modes and utilizes a new phase detecting structure to achieve inherent cancellation of internal phase offset. The proposed digital FMDLL is implemented in a 65-nm 1-V CMOS process and occupies an area of 0.019 mm^2 with programmable frequency ratios of N = 1, 4, 5, 8, 10 and M = 1, 2, 3. It operates over a frequency range of 0.7–2.0 GHz and achieves an effective peak-to-peak (p-p) jitter of 10 ps at 2 GHz when N/M = 8/2. It achieves a locking time of only 40 clock cycles and dissipates 3.3 mW at 1 GHz when N/M = 1/1. The FMDLL employs a new harmonic lock detector to eliminate the harmonic lock problem and achieve dynamic switching of the clock frequencies and division ratios.

Jongsun Kim from 1994 to 2001, Dr. Jongsun Kim was with Samsung Electronics as a senior research engineer in the DRAM Design Team, where he worked on the design and development of Synchronous DRAMs, SGDRAMs, Rambus DRAMs, and other specialty DRAMs. He received the Ph.D. degree from the Electrical Engineering Department, University of California, Los Angeles (UCLA) in 2006. He was a Postdoctoral Fellow at UCLA from 2006 to 2007. After his research at UCLA, he returned to South Korea to continue his memory design career at Samsung, where he was in charge of developing the next generation high-speed DDR4 DRAMs. Dr. Kim joined the School of Electronic & Electrical Engineering, Hongik University in March 2008. Prof. Kim's research interests are in the area of high-performance mixed-mode (analog & digital) circuits and systems design. His current research areas include high-speed and low-power transceiver circuits for chip-to-chip communications, clock recovery circuits (PLLs/DLLs/CDRs/SerDes), frequency synthesizers, low-power and high-bandwidth memories (DRAM/FLASH), power-management ICs (DC-DC converters), deep-learning circuits and systems, low-power neuromorphic circuits for AI, and low-power sensors and transceivers for IoT. He is a member of IEEE, IEIE, IEICE, and ISE.

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Low-Power Small-Area Direct Digital Frequency Synthesizers

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Direct-digital frequency synthesizers (DDFSs) have been employed in many frequency-agile communication systems because of their wide bandwidth, fine frequency resolution, and fast frequency hopping characteristics. However, they still have disadvantages in power, size, and spectral purity. In this talk we will discuss about a high efficiency DDFS designed to enhance power dissipation, size, and spectral purity. Starting with a general introduction of DDFS, the following key ideas for enhancing the overall performances of the DDFS will be discussed. (1) Multi-level momentarily activated bias for reducing power dissipation in phase accumulator; (2) Coarse phase-based consecutive fine amplitude grouping scheme for reducing the hardware complexity and the power consumption in decoder circuits; (3) Mixed-wave conversion topology in the nonlinear DAC for higher spectral purity.

Kwang-Hyun Baek received the B.S. and M.S. degrees in electronics engineering from Korea University, Seoul, Korea, in 1990 and 1998, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Urbana, IL, USA, in 2002. From 1990 to 1996, he was with Samsung Electronics, and he was with the Department of High-Speed Mixed-Signal ICs as a Senior Scientist at Rockwell Scientific Company, formerly Rockwell Science Center (RSC), Thousand Oaks, CA, USA, from 2000 to 2006. At RSC, he was involved in the development of high-speed data converters (ADC/DAC) and direct digital frequency synthesizers (DDFS). Since 2006, he has been with the School of Electrical and Electronics Engineering, Chung-Ang University, Seoul, Korea.

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A Survey on Memristor Circuits and Systems for Brain-Inspired Computing

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With the recent advanced in memristor as a potential emerging device for future technique, it becomes interesting and timely topic to study the applications of memristor. To address this issue, this paper presents a survey on research activities of memristor in brain-inspired computing system. This paper reviews the memristor logics, where the computation and memory can be merged together. Then, we introduce neuromorphic memristor crossbars which can mimic the brain's pattern recognitions of speech and image. The simulation results of neuromorphic crossbars strongly highlight the future possibility of memristor circuits in brain-mimicking pattern processing.

Son Ngoc Truong received the B.S. and M.S. degrees in Electronic Engineering from The University of Technical Education Ho Chi Minh City, Vietnam, in 2006 and 2011, respectively, and the Ph.D degree in Electronic Engineering from Kookmin University, Seoul, Korea, in 2016. He was a research assistant at Kookmin University, Seoul, Korea in 2016 and 2017. His current research interests include Neuromorphic computing system, Brain-inspired system.

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A Novel Memristor Crossbar Architecture Based Multilayer Neural Network for Speech Recognition

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A novel binary memristor crossbar architecture based on multilayer neural networks is proposed for speech recognition application. Here, the memristor crossbar circuit acts as the weights of the neural network combined with the activation function circuit to determine the output. In the new crossbar architecture, the weights are arranged diagonally and divided into 2 arrays according to positive and negative weights. A speech recognition application for 5 vowels is implemented using the proposed architecture. The result shows that the average recognition rate achieves from 94% to 96.6% over 1000 audio samples. A statistical table shows that the recognition rate and the number of the memristors increase correspondingly to the number of used bits. From the Monte Carlo simulation, the recognition rate of the proposed binary memristor crossbar is decreased slightly from 94% to 93.7%, while the memristance variation is increased from 1% to 15%.

Minh Huan Vo received the B.S. and M.S.E.E. degrees in Electronics and Communication Engineering from the Ho Chi Minh City University of Technology, Vietnam in 2005 and 2007 and Ph.D. degree in Electronics Engineering from Kookmin University, Seoul, Korea in 2013. He is currently working as a lecturer at the Faculty of Electrical and Electronics Engineering, University of Technology and Education, Ho Chi Minh City, Vietnam. His current research interests include low power design optimization in VLSI and IoT system and neuromorphic computation using emerging technology like memristive devices.

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Parking Space Detection upon a Deep CNN and Multi-task Contrastive Network Spatial Transform"

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Nowadays, deep learning methods, especially CNNs, have achieved many promising results in a wide range of computer vision applications. However, few studies focused on designing suitable deep learning methods for parking space status inference. As we have known, it is challenging to detect parking spaces in an outdoor environment due to dynamic lighting variations, weather changes, and perspective distortion. By off-the-shelf CNNs, lighting variations might be handled well. However, to realize a practical and robust inference system, we also need to address troublesome problems such as parking displacements, non-unified car sizes, inter-object occlusion, and perspective distortion. These problems may become even challenging if also considering the difference of space sizes. To overcome the problems, we proposed a custom–tailored deep convolutional and contrastive network with three contributions. First, we introduced a Siamese architecture to learn the contrastive and robust feature descriptor. This helps to reduce the effects owing to the variety of inter-object occlusion. Second, we integrated a convolutional Spatial Transformer Network (STN) to adaptively transform a 3-space input patch according to vehicle sizes and parking displacement. STN also helps to overcome the perspective distortion problem. Third, a multi-task loss function was designed to train the network by simultaneously considering the accuracy of inferring the status of the target space and the semantic smoothness of high-level features. Thereby, the errors caused by inter-object occlusion could be alleviated. To verify the proposed network, we visualized the learned features and analyzed their functionality. Experiments and evaluations have shown the robustness of our system in parking status inference. The real-time system currently running in public parking lots also demonstrates the effectiveness of the proposed deep network.

Vu-Hoang Tran received the B.S. degree in Electrical Engineering from Ho Chi Minh City University of Technology and Education, Vietnam in 2012, the Master degree from National Kaohsiung University of Applied Sciences, Taiwan, in 2015, and the Ph.D. degree from National Chung Cheng University, Taiwan, in 2018. He is currently a lecturer in Ho Chi Minh City University of Technology and Education, Vietnam. His research interests are in image processing, pattern recognition, computer vision, machine learning, and transfer learning.

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Innovative assessment metrics for upper limb robot-assisted rehabilitation"

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Upper limb disability following stroke affect activities of daily living and can drastically change the stroke survivors life. To enhance the quality of life for stroke survivors, rehabilitation plays a key role for the patient to regain motor and cognitive function. Robot-assisted training has been demonstrated to provide a safe, effective and cost-effective approach for upper limb rehabilitation. The motor recovery evaluation using clinical outcome measures is usually performed before and after the training: evaluation during training can be difficult because of time and resources limitation. The use of kinematic parameters in addition to clinical scales as evaluation tools is proposed. However, the identification of the most appropriate clinical outcome measures and kinematic parameters to be used as an integrated assessment method is still being debated.

I will report on two clinical trials, to investigate the application of an integrated evaluation approach which combines clinical outcome measures, kinematic parameters, for motor recovery assessment following robot-assisted training. The proposed evaluation method is expected to provide a comprehensive and detailed evaluation of the recovery of the patient, not only before and after but also during the training, such as after each single training session.

The results from the two trials showed that the kinematic parameters provide objective measures about patient motor performance. The combined use of kinematic parameters and clinical outcome measures represents reliable, useful and easy to be delivered approach for motor recovery assessment following robot-assisted rehabilitation.

Tran Vi Do received the Ph.D. degree in Biorobotics from the BioRobotics Institute, Scuola Superiore Sant'Anna di Pisa, Italy in 2018. Currently, he is Lecturer of Automatic Control Department at the Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education, Vietnam.
His research interests are in the fields of rehabilitation robotics, assistive technologies and human-robot interaction.

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Control System with Smart Phone for the Mini Aquaponics Cabinet

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With the rapid urbanization in large cities today, agricultural land is gradually giving way to high-rise buildings and transportation works. Therefore, finding or building a vegetable garden, a clean fish tank, keeping ecological balance of living environment in the city is a major concern of the country.

The demand for clean, green food and international standards is always set for the farmer to be able to bring agricultural products to the table family and restaurants. Many countries have been successful in the field of high-tech agriculture with the export of agricultural products and technologies for growing vegetables and aquatic and marine products.

In addition, with the current technological and IoT success, we can apply radical models of agriculture to increase labor productivity and harvest high quality agricultural products of life. Many research group and farmers try to contribute a small part to solve the above problems.

In this work, the aquaponics cabinet was made and operated as well as the following information in below:

- Using the microcontroller of Arduino for the control systems and sensors
- Get the live environment parameters by sensors: temperature, humidity, and light intensity
- Can be show the graph on the smartphone
- Control electronic devices from smartphone by using the automatic mode of operation.

And other functions.

The mini aquaponics cabinet works stably and displays environmental parameters (air temperature, humidity, LED illumination, …) and can be used to control the opening and closing of the fan by the smart phone. Both lettuce and fish are being tested by hydroponics on the mini aquaponic cabinet. Processor control and remote control system, remote Wi-Fi connection has made the system dynamic. The mini aquaponic cabinet promises to be a miniature "pond of vegetables and fish" in the living room or in the public area.

Nguyen Van HIEU received his bachelor and master degree in Ho Chi Minh City University, Vietnam (1994 and 2000). He obtained his PhD degree in Graduate School of Science, Osaka University (Japan, 2007). In 2010, he was invited as visiting professor in Ritsumeikan University, Japan. He was also invited as researcher for the Lab of Semiconducting technology (Saigon Hi-Tech Park, since 2011). From Dec 2008 to Sep 2010, he served as Dean of Faculty of Electronics and Telecommunications. He was appointed an associate professor in 2011. In 2017, he had the lectures and joint research works as an inviting research Associate Professor in Sophia University, Tokyo, Japan. Now, he is associate professor and head of Dept. of Physics and Electronics Engineering (VNU Ho Chi Minh City- University of Science).

His current research topics are the semiconducting devices, the applied electronics engineering and the application of high-tech in agriculture

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Coronary Vessel Segmentation by Coarse-to-Fine Strategy using Otsu Algorithm and Decimation-Free Directional Filter Bank

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In this study, a novel approach is investigated to extract coronary vessel from X-ray angiogram. First, we propose to combine Decimation-free Directional Filter Bank (DDFB) and Homographic Filtering (HF) in order to enhance X-ray coronary angiographic image for segmentation purposes. This approach not only enhances the vessels at different orientation and radius but also simultaneously normalizes the brightness across the image and increases contrast. Next, a coarse-to-fine strategy for iterative segmentation based on Otsu algorithm is applied to extract the coronary vessels in different sizes. Experimental results on our coronary X-ray angiography dataset demonstrate that the proposed approach can outperform the standard method and attain the accuracy of 71.34%.

Pham The Bao received his bachelor, master degree in 1995 and 2000, respectively. He also obtained his Ph.D. degree at University of Science in 2009. From 1995 to 11/2018, he was a lecturer in the Department Computer Science, Faculty of Mathematics & Computer Science, University of Science, Hochiminh city, Vietnam. From 11/2018 until now, he is working as a lecturer in the Department Computer Science, Faculty of Information Science, Sai Gon University, Hochiminh city, Vietnam. His research interests include Image processing & pattern recognition, intelligent computing.

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Wireless Sensor Networks for the Internet of Things

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Wireless Sensor Networks (WSNs) are now widely diffused in different applications, such as military, agriculture, sports, medicine, industry and many civilian application scenarios, including home and building automation, health monitoring, environment monitoring, traffic control, … Currently, WSNs are an integral part of the Internet of Things (IoT) system. Applications in the IoT system require for low cost, low power, high number of sensors, fast deployment, long life-time, low maintenance, and high quality of service. Many technologies have been researched and developed to meet the above requirements, such as ZigBee, Bluetooth, WiFi, GPRS/3G/4G, Long Range Radio (LoRa). In which, LoRa is a wireless telecommuni-cations system, promoted as an infrastructure solution for the IoT. In this report we focus on the research and design of a WSN for IoT applications (such as smart city and smart agriculture) based on LoRa technology.

Nguyen Chi Nhan received his B.S. and M.Sc. degrees in Physical Electronics from University of Science, Vietnam National University - Ho Chi Minh City (VNU-HCMC), in 1999 and 2004, respectively. He joined the internship program for Ph.D. course at the Department of Electrical and Computer Engineering, University of Saskatchewan, Canada, from August 15, 2011 to January 18, 2012. He received his Ph.D. degree in Physics and Electronics at University of Science, VNU-HCMC, in 2016. His research field of interest includes wireless communications (RF, UWB), VLSI Design, Integrated Circuit Design and Embedded System.

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Thermal Energy Harvesting Circuit for Wearable Applications

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In this paper, we design a thermal energy harvesting circuit for wearable applications and propose low-power operational methods for the energy-harvesting sensor and touch-panel circuits. Here, the amount of harvested current has been measured as low as 8uA due to a very small difference between the human body and environmental temperatures. However, the power consumption of the sensor and touch-panel circuits is known to consume much larger than 8uA. Thus, we need to have the hardware-based power-gating or the software-based active/sleep scheme, for suppressing the power consumption of sensor and touch-panel circuits lower than a target limit. In the hardware-based power-gating scheme, if the ratio of off-time/on-time is larger than 22, the sensor can consume less than 8uA. For the software-based active/sleep control scheme, if the ratio of sleep-time/active-time is larger than 3, we can suppress the current consumption below the target limit. The hardware-based and software-based schemes studied in this work would be helpful in various wearable applications of energy-harvesting sensor and touch-panel circuits, where the power consumption should be limited by an amount of harvestable energy from the thermal electric generator.

Kyeong-Sik Min received the B.S. degree in Electronics and Computer Engineering from Korea University, Seoul, Korea, in 1991, and the M.S.E.E. and Ph. D. degrees in Electrical Engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1993 and 1997, respectively. In 1997, he joined Hynix Semiconductor Inc., where he was engaged in the development of low-power and high-speed DRAM circuits. From 2001 to 2002, he was a research associate at University of Tokyo, Tokyo, Japan, where he designed low-leakage memories and low-leakage logic circuits. In September 2002, he joined the faculty of Kookmin University, Seoul, Korea, where he is currently a Professor in the School of Electrical Engineering. He was a visiting professor at University of California, Merced, from Aug. 2008 to July 2009. Prof. Min served on various technical program committees such as Asian Solid-State Circuits Conference (A-SSCC), International SoC Design Conference (ISOCC), and Korean Conference on Semiconductors (KCS). He and his students received IDEC CAD & Design Methodology Award (2011), IDEC Chip Design Contest Award (2011), and IDEC Chip Design Contest Award (2012). He is a member of Institute of Electrical and Electronics Engineers (IEEE), Institute of Electronics Engineers of Korea (IEEK), and Institute of Electronics, Information, and Communication Engineers (IEICE) in Japan. His research interests include low-power VLSI, memory design, and power IC design.

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(POSTER PRESENTATION)

The Circuit Setting-up Irradiation Time for Photolithography Process using Arduino Microcontroller

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The micro controller Arduino Uno were used to set up the time of UV irradiation for the lithography steps for wafer as Fig.1 in below:
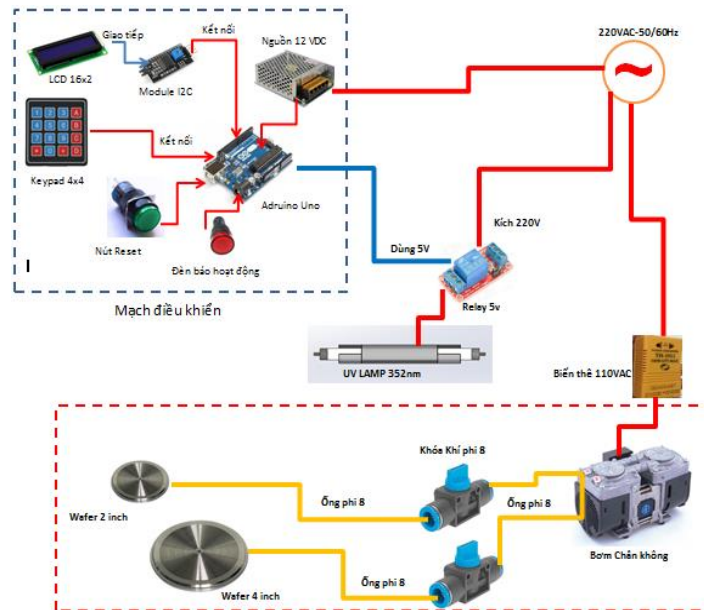

Figure 1 The description of electronic devices and equipments to control by microprocessor Arduino của the mini lithography cabinet.

The control circuit for UV irradiation time is described and operated as follows:-
- Module 12C link displays information via LCD.
- Keypad to enter the irradiation time.
- Reset button when needing to restart the system.
- 220V source is supplied for honeycomb source to supply 12VDC for Arduino Uno processor.
Principles to control the interrupt time and open UV irradiation are as follows:
. 5VCD power from the Arduino processor adds to the relay opening and closing over the time set by the processor
. When relay opens, 220VAC source is granted to UV lamp to irradiate UV until relay is closed, irradiation is finished.
 In addition, the vacuum pump is powered by 100V (transformer from 220V) to create a gas stream that draws the wafer tightening bases. The attraction of this pump can be controlled by two hand valves to adjust the force that we want to hold the wafer.
The system has been working stably, well controlling the photolithography of electrode shapes to study the technology of manufacturing UVLED electrodes.
Key words: Arduino, UV lamp, photolithography, UVLED electrodes.

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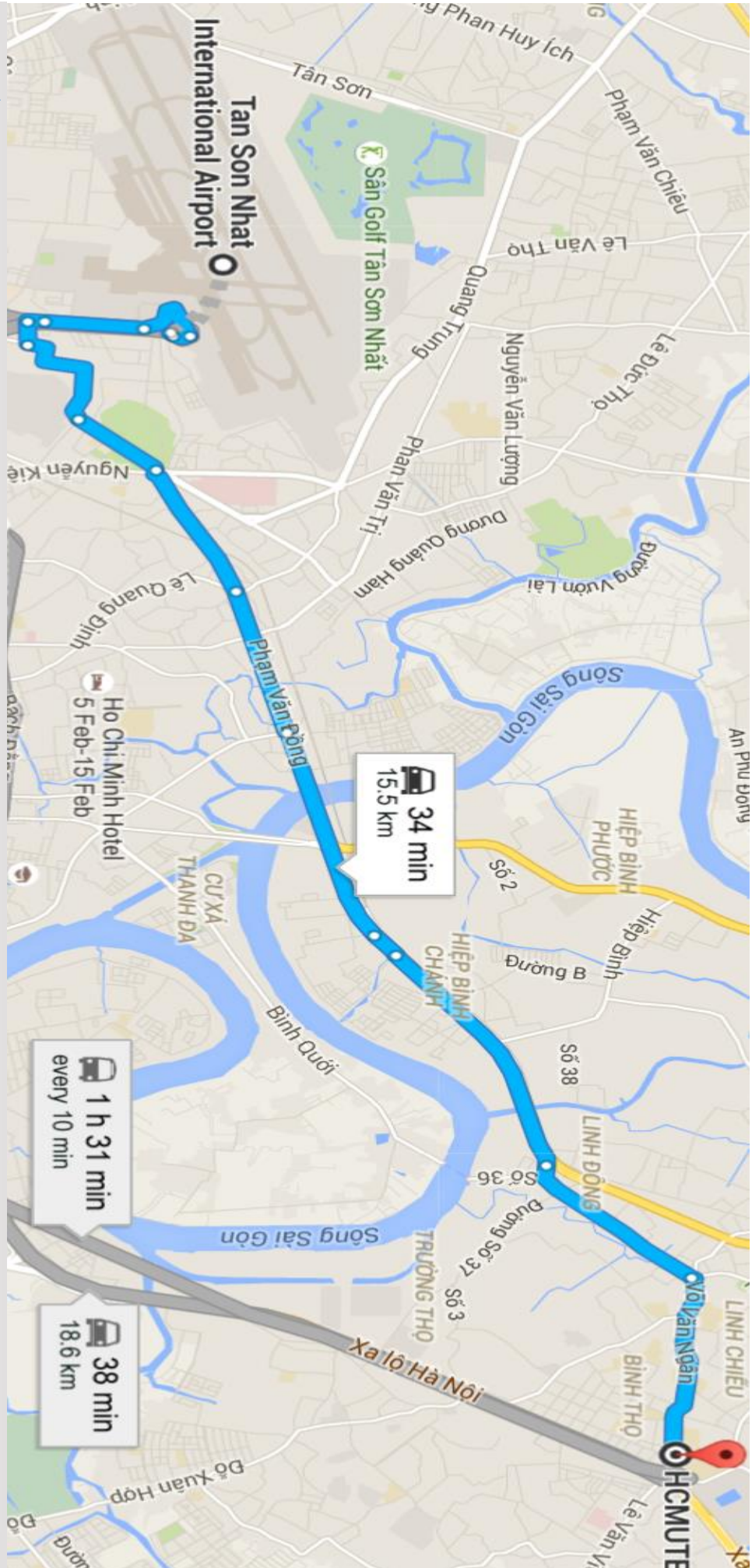
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1: Main Entrance
2: Sub Entrance
3: Main Building
(Meeting room 2, 6 th floor)
4: Parking lot
5: A block
6: B block
7: C block
8: D block
9: Viet Duc Block
10: Stadium
11: Super market
12: Car parking